AMENDMENTS TO THE CLAIMS

1. (Previously Presented) An interconnect structure, comprising:

a plurality of interconnected nodes, including distinct nodes A and E;

the node A having a plurality of data input ports, a plurality of data output ports, and a control signal input port; and

the node E having a plurality of data input ports, a plurality of data output ports, and a control signal output port; and

a routing logic associated with the nodes, the routing logic for routing data selectively among the interconnected nodes;

the nodes A and E being positioned in the interconnect structure so that node A cannot route data to the node E, the node E cannot route data to the node A, and no node exists in the interconnect structure that can have data routed directly to it from both the node A and the node E; and

a logic included as part of said routing logic and associated with the node A that uses information concerning routing of data through the node E to route data through the node A.

2. (Previously Presented) An interconnect structure in accordance with Claim 1 wherein:

the plurality of interconnected nodes includes a node F distinct from the nodes A and E, the node F having a plurality of data input ports, a plurality of data output ports, and a control signal output port; and

the nodes A and F are positioned in the interconnect structure so that the node A cannot route data to the node F, the node F cannot route data through

the node A, and no node exists in the interconnect structure that can receive data directly routed both from the node A and the node F; and

the logic associated with the node A uses information concerning routing of data through the node F to route data through the node A.

3. (Original) An interconnect structure in accordance with Claim 2 wherein:

the plurality of interconnected nodes includes a node B distinct from the nodes A, E and F, the node B having a plurality of data input ports, a plurality of data output ports, and a control signal output port; and

a logic associated with node B included as part of the routing logic being capable of sending a control signal z to the node A, the control signal z containing information concerning routing possibilities through the nodes B, F and E, and the logic associated with the node A for routing of data through the node A depending at least in part on information concerning routing of data through the nodes B, F and E.

4. (Original) An interconnect structure in accordance with Claim 3 wherein:

the plurality of interconnected nodes including a node C distinct from the nodes A, B, E, and F, the node C having a plurality of data input ports, and a plurality of data output ports;

the node B sends a message to the node C;

the node E sends a control signal y to the node B;

the node F sends a control signal x to the node B;

the logic associated with the node B sends a non-blocking control signal z to the node A based on the control signals x and y;

the node A sends a message to the node C; and

the node C simultaneously receives messages into all of its input ports.

5. (Previously Presented) An interconnect structure comprising:

a plurality of nodes including distinct nodes A, B and C, the nodes A and B being both positioned to send data to the node C;

a plurality of interconnect lines selectively coupling the nodes of the interconnect structure;

a control signal carrying line connected from the node B to the node A for carrying control signals from the node B to the node A; and

a routing logic associated with the node B capable of sending data to the node C and sending a control signal to the node A that can inform the node A that the node A is allowed to send a message to the node C.

6. (Previously Presented) An interconnect structure in accordance with Claim 5 wherein:

the node C has a plurality of input ports; and

data from the nodes A and B arrive at the node C concurrently so that all [[N]] of the input ports of the node C receive messages simultaneously.

7. (Previously Presented) An interconnect structure in accordance with Claim 6 wherein:

the plurality of nodes includes distinct nodes A, B, C, D, E, F and H; and

the node C is capable of simultaneously sending data from the node A to the node D, and capable of sending data form the node B to the node H.

8. (Currently Amended) An interconnect structure in accordance with Claim 7 wherein:

the interconnect structure is hierarchical;

the node A is on a level of the hierarchy;

the nodes E, B, C, and D are on the level of the hierarchy directly below the level of the node A; and

the nodes [[E,]] F and H are on a level of the hierarchy directly below the level of the node B.

9. (Currently Amended) An interconnect structure comprising:

a plurality of nodes adapted to generate control signals including the distinct nodes A, B, and C, and a collection of interconnect lines selectively coupling the nodes;

the node C having a plurality of message input ports, the nodes A and C positioned in the structure so that A can route a data packet to C;

the nodes B and C positioned in the structure so that B can route a data packet to C;

the nodes A and B positioned in the network so that B can send a control signal to A;

[[the]] a routing logic at the node A using the control signal from node B to route messages;

the node B routing a message MB to C;

the node A routing a message MA to C to arrive at concurrently with MB;

all input ports of C concurrently receiving a message.

10. (Canceled)

11. (Currently Amended) An interconnect structure in accordance with claim [[10]] 16, wherein said routing logic assumes that message MB is not blocked from using the first output port and message MA is not blocked from using the second output port.

12. (Previously Presented) An interconnect structure in accordance with claim 11, wherein said routing logic for the routing of messages MA and MB depends in part on QOS criteria.

13. (Currently Amended) An interconnect structure comprising:

a plurality of interconnected nodes including nodes A, B, C, D, and H, each of the nodes A, B, C, D and H having a plurality of input ports and a plurality of output ports, and node C being positioned to receive messages from A and B and to route messages to D and H;

a plurality of interconnect structure output ports including [[the]] an output port that is accessible from node C but not node H;

a routing logic included within the interconnect structure to assure that when node A sends a message MA to node C and concurrently node B sends a message MB to node C, then node C can route MA through node D to a target interconnect structure output port for MA and node C can route MB through node H to a target interconnect structure output port for MB.

14. (Previously Presented) An interconnect structure in accordance with claim 13, wherein said routing logic assures that message MB is not blocked from node H, and message MA is not blocked from node D.

15. (Original) An interconnect structure in accordance with claim 14, wherein said routing logic is responsive to QOS criteria.

16. (New) An interconnect structure comprising:

a plurality of interconnected nodes including a node C having input ports I_A and I_B and output ports O_H and O_D;

all output ports accessible from I_A being accessible from output O_D;

a plurality of output ports that are accessible from input port I_B but not from output O_H; and

a routing logic included within the interconnect structure to assure that when a message M_A arrives at input port I_A and simultaneously a message M_B arrives at input port I_B there is a path through output port O_D to a target destination for message M_B.

17. (New) An interconnect structure for carrying message packets consisting of a header and a payload with header indicating a target output port comprising:

a plurality of interconnected nodes including a node C having input ports I_A and I_B and output ports O_H and O_D;

a plurality of output ports that are accessible from input port I_B but not from output O_H; and

a routing logic included within the interconnect structure to assure that when a message M_A arrives at input port I_A and simultaneously a message M_B arrives at input port I_B there is a path through output port O_D to a target destination for message M_B and a path through output port O_H to a target destination for message M_B.

18. (New) An interconnect structure in accordance with claim 17, wherein said routing logic assumes that message MB is not blocked from using the first output port and message MA is not blocked from using the second output port.